Applicant : Jeff Cuppett et al
Patent No. : n/a
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Page : 6

Attorney's Docket No.: 00121-003100000:

REMARKS

In the office action mailed September 3, 2008, the Examiner rejected claims 1-6, 9-11 under 35 USC 112 for not pointing out and distinctly defining the subject matter the Applicant regards as his invention. Specifically, the Examiner indicated "it is not clear to the Examiner how the gates are configured in hardware to validate format/command or what the structure of gates is." The Examiner asserted that it "is also not clear to the Examiner how the gates are configured in hardware to effect format/command validation at wire speed." Applicant has modified the claims to clarify how gates are configured to validate both a "format" of a frame as well as a "command" associated with a frame.

Claim 1 as amended recites a circuit having "one or more gates corresponding to a number of bits to be validated" in order to emphasize that any number of bits in a frame or multiple frames may validated simultaneously. (See paragraph [0035] of the specification) Applicant respectfully submits that many different structures of the gates are possible provided they allow for bit by bit comparisons. Moreover, validating formats and commands with multiple gates corresponding to the number of bits allows the validation process to operate a "wire speed".

Applicant respectfully submits that the aforementioned modifications sufficiently clarify aspects of the invention and therefore the rejection of Claim 1-6 and 9-11 under 35 USC 112 2nd paragraph should be withdrawn.

Further, the Examiner rejected Claims 1-6 and 9-11 under 35 USC 102(e) in view of U.S. Patent 6,728,861 to Roach et al. (hereinafter "Roach"). Applicant respectfully submits that Roach

cannot anticipate Claim 1 as it does not teach every limitation recited in Claim 1. First, Roach begins by separating a received frame into header and payload components. (Col. 2, lines 34-36 of Roach) The header data and 1st eights words of the frame payload are split off and stored in a first memory (i.e., Header & Payload RAM). (Col. 2, lines 37-41) Next, the payload is then separately stored in a second memory (i.e., local memory). (Col. 3, lines 41-47 of Roach) Frame validation results are placed in yet another third memory (i.e., Completion RAM). (Col. 3, lines 59-64 of Roach). Because the frame is split into two separate portions, it is impossible for Roach to both "validate format information including in a frame of data" as well as "validate command information included in the [same] frame of data" as recited in Claim 1.

Indeed, Roach uses a third memory (i.e., Completion RAM). (Col. 3, lines 59-64 of Roach) to store frame validation results rather than writing error information "in the frame of data if an error is found in the format information" as recited in Claim 1. It also follows that Roach fails to write error information "in the frame of data if an error is found in the command information" as also recited in Claim 1. Because Roach stores validation results in a third memory and not inside the frame of data then it is not possible to pass error information in a common frame being processed as recited in Claim 1.

Applicant respectfully submits that Claim 1 remains in condition for allowance and therefore dependant Claims 2-6 are also in condition for allowance by virtue of their dependency on Claim 1. Independent Claim 9 is at least in condition for allowance for similar reasons as Claim 1. Likewise, Claims 10-11 are also in condition for allowance by virtue of their dependence on Claim 9.

The Examiner also rejected Claims 1-6 and 9-11 under 35 USC 102(b) in view of software validation systems mentioned in the "Background" section of the Applicant's application (hereinafter "Software validation"). Applicant mentioned that software code has been used to

validate frames yet this also does not anticipate Claim 1. Software validation performs various conditional branches and other comparisons that take a longer period of time. These software validations mentioned in the background do not "validate format information included in a frame of data with simultaneous bit by bit comparisons" as recited in Claim 1. Software validations mentioned in the background also do not "validate command information included in the frame of data with simultaneous bit by bit comparisons" as also recited in Claim 1.

Software validation mentioned in the background of the Application also makes no mention of how validation results or error information is handled. Accordingly, it is not possible for Software validation from the background section to anticipate Claim 1 because Software validation does not have "error information is written in the frame of data if an error is found in the format information" as recited in Claim 1. Likewise, the Software validation also does not have "error information is written in the frame of data if an error is found in the command information" as recited in Claim 1.

For at least these additional reasons, Applicant respectfully requests withdrawal of the rejection of Claim 1 and Claim 9. Dependent Claims 2-6 and 10-11 depend from Claim 1 and Claim 9 respectfully and also in condition of allowance for at least the same reasons previously provided.

Further, the Examiner rejected claims 1-6 and 9-11 under 35 USC 103(a) as obvious in view of Software validation or Applicant's Admitted Prior Art and further in view of U.S. Patent 6,356,944 to McCarty (hereinafter McCarty). First, Software validation mentioned in the Background of the Application does not teach or suggest several aspects of Claim 1 as previously mentioned. Adding hardware for error detection from McCarthy also does not address the larger concern that Software validation does not scale to larger proportions. Software validation does not

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Page : 9

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operate by having "error information is written in the frame of data if an error is found in the command information" as recited in Claim 1.

For at least the aforementioned reasons, Claim 1 is in condition for allowance. Claim 9 is also in condition for allowance for similar reasons. Claims 2-6 depend from Claim 1 and also remain in condition for allowance.

Accordingly, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Leland Wiesner, Applicants' Attorney at (650) 853-1113x101 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

Leland Wiesner

__2/3/2009_____ Date

____/Leland Wiesner/_____
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